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Efficient and Bidirectional Cascaded Auxiliary Power Module Design for Electric Trucks Using Hybrid Si, SiC, and GaN Technologies

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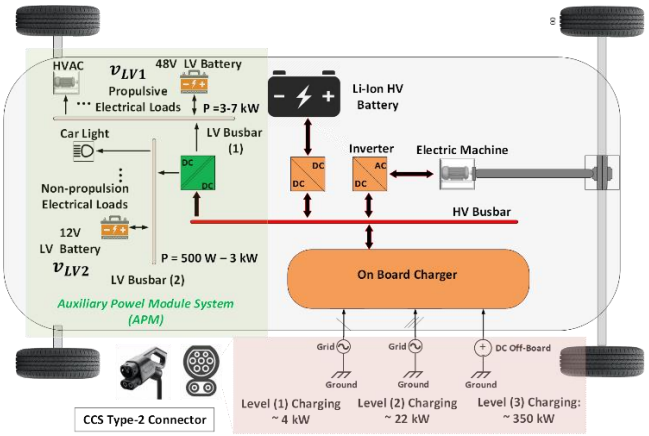
***Abstract*—In battery electric vehicles (BEVs), ensuring reliable auxiliary power is crucial for supporting essential functions such as communications, cooling systems, cabin air conditioning and emergency braking. Traditionally, 12V batteries have been widely used for auxiliary systems, but there is now a shift towards 48V systems, driven by the need for improved vehicle efficiency and enhanced performance. This transition is significant, especially for future medium and heavy duty BEVs, which are expected to use multiple low-voltage (LV) batteries to optimize power distribution. As part of an EU H2020 project, it is required to develop a digital twin model of the auxiliary loads power supply for an electric Truck. Hence, this research focuses on providing a proof of concept validation for an isolated DC-DC converter, known as the auxiliary power module (APM) through a high-fidelity model. This paper presents the design and evaluation of a single-input, multi-output cascaded APM topology for electric trucks, emphasizing its efficiency and performance. The integration of advanced switching technologies, including Si and SiC MOSFETs and GaN HEMTs, is highlighted for their potential to enhance APM functionality. A high-fidelity co-simulation model has been developed using PLECS-Blockset and MATLAB Simulink, demonstrating the APM's ability to achieve a peak efficiency of 98% at 10 kW in bidirectional power control between the high voltage (HV) bus and two LV buses.**

***Keywords*— EV, isolated DC-DC converter, Auxiliaries power module, Cascaded DC-DC, Single-input-multi-output, Dual active bridge converter, and Buck-boost converter.**

I. INTRODUCTION

As part of the European Union (EU) plan for the fundamental transport transformation to an ecologically friendly system, the manufacturing industry of BEVs has been showing huge transformations [1]. In addition to that, the Russia-Ukraine conflict significantly boosted the sales of BEVs in China, thereby positively influencing the country's automotive energy structure [2], [3]. The energy demand of various auxiliary systems and components in electric trucks (ETrucks), such as heating, ventilation, and air conditioning (HVAC) systems, power steering, and other onboard electronics is also evolving. Every ETruck relies on at least one LV battery to power these auxiliary loads. Typically, the standard LV battery is 12V. However, the recent trend is to shift to 48V in the LV system, especially for ETrucks, to minimize power losses in the extensive wiring within the vehicle [3], [4]. The integration of 48V and 12V batteries has become standard in mild-hybrid trucks like the Daimler Super Truck II [5], [6].

Future ETrucks will also require an APM to supply power from the HV battery to both 48V and 12V LV batteries. The 12V system will support low power loads (500W-3kW) such as the HV system start circuit and onboard computer system, while the 48V system will handle higher power loads (3-7 kW) [3]. This requires an efficient and modular APM design, that facilitate bidirectional power transfer control between the HV bus and two LV buses. This solution will increase the ETruck reliability in case of HV battery failure. Figure 1 illustrates the principal architecture of the proposed APM system.



Principal architecture of innovative Single-input-multi-output APM in ETrucks as part of an EU H2020 project

This paper examines a 10 kW rated two-stage cascaded topology for an APM system from the efficiency point of view. The first stage employs an isolated Dual Active Bridge (DAB) topology to step down from the HV bus to the 48V bus (LV1), while the second stage utilizes a non-isolated buck-boost topology to step down from the 48V bus to the 12V bus (LV2). By incorporating Si MOSFETs and wide bandgap (WBG) semiconductors such as SiC MOSFETs and GaN HEMTs, this design aims for high efficiency at elevated currents and high switching frequencies. The increased switching frequency results in reduced passive

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component size and increased power density. A high-fidelity co-simulation model has been developed using PLECS-Blockset and MATLAB Simulink to evaluate the design performance under various operating conditions.

The paper is organized as follows: Section II details the conceptual design of the APM and outlines the benefits of using Si MOSFET, SiC MOSFET, and GaN HEMT technologies. Section III presents the design of the DAB converter stage. Section IV discusses the design of the buck-boost stage. Section V provides the analysis and simulation results, and Section VI concludes the study.

II. Conceptual Design of APM System

A. Selection criterion of cascaded topologies

The main system requirements of an ETruck on-board APM include galvanic isolation between HV and LV buses, minimal peak-to-peak voltage ripples on the HV and LV buses, high efficiency, and high power density. The DAB converter topology is suitable for the first step-down stage from the HV bus to the 48V bus, as it meets all these requirements [3]. The DAB converter includes a transformer for galvanic isolation and ensures zero voltage switching (ZVS), which enhances efficiency at high switching frequencies. Additionally, the DAB allows for easy bidirectional power flow control between the HV and 48V buses [3], [7].

For the second step-down stage from 48V to 12V, a non-isolated synchronous interleaved buck-boost topology is chosen due to its simplicity as a bi-directional converter. To further improve the current ripples in the inductor, a two-phase interleaved buck-boost topology has been adopted. The normal operating mode is the buck step-down mode, converting from the 48V battery to the 12V battery. However, in scenarios where the 48V battery voltage drops to critical levels (e.g., 36V), the converter can switch to boost mode and charge the LV1 bus from the LV2 bus. Figure 2 shows the proposed APM topology.

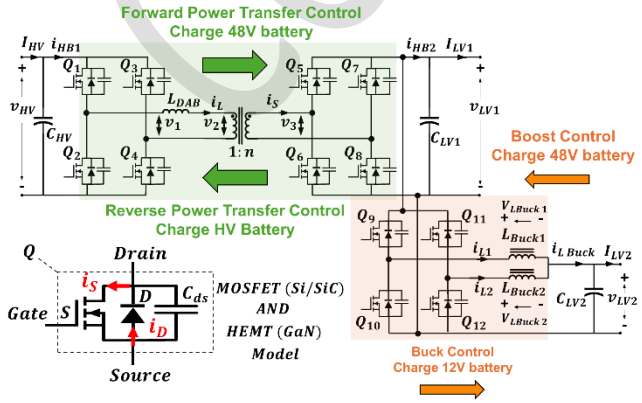

Fig. 1. Proposed APM cascaded topology with DAB converter in HV/48V stage and Buck-boost converter in 48V/12V stage.

B. Operating modes of the APM

In this paper, a 700V, 200 kWh ETruck HV battery has been selected for the evaluation of the APM performance. The 700V system in ETrucks enhances efficiency and supports faster charging. However, high-frequency step-down transformers with large step-down ratios, face challenges like increased insulation requirements, and complex thermal management. The simulation examines the performance of the APM at different charge conditions of the HV battery, specifically at nominal voltage (700V), maximum voltage (730V), and minimum voltage (550V).

For the 12V battery, the nominal voltage in an open circuit or fully charged state with the vehicle off (resting mode) is 12.7V, which can drop to 11V before the BMS disconnects the battery from the LV network. During vehicle operation, the APM maintains the LV battery voltage between 13.5V and 14.3V. For the 48V battery system, the resting voltage is 52V when fully charged, with a minimum BMS voltage of 40V and a normal operating range of 48V to 52V [8] , [9], [10] .

The system experiences minimum fast voltage dip levels of 9V for the 12V bus and 36V for the 48V bus upon startup. In evaluating the DAB converter's operation, we will consider the extreme voltage values of 36V, 48V, and 54V to ensure comprehensive performance analysis under various critical conditions.

C. Selection of Si MOSFET, SiC MOSFET and GaN HEMT technologies in the APM application

For the DAB stage primary H-Bridge, it is important to select semiconductor switches with high breakdown voltage capabilities [11]. Therefore, SiC MOSFETs are suitable for the primary H-Bridge due to their high efficiency and good thermal performance at high switching frequencies. For the secondary H-Bridge, semiconductors with high current carrying capabilities and low breakdown voltage are beneficial. This can be achieved with either Si MOSFETs or GaN HEMT switches; however, GaN HEMTs are more suitable for high switching frequency applications above 100kHz, and it has higher cost. Thus, Si MOSFETs are selected for the secondary H-Bridge. For the Interleaved Buck-Boost converter, GaN HEMT switches are selected to maximize power density by increasing the switching frequency beyond 100kHz while ensuring low losses and stable thermal performance.

III. Design and Operation of DAB Converter

A. Power flow control concept of DAB

As shown in Figure 3, the DAB converter comprises two H-bridges on the primary and secondary sides of a high-frequency transformer with a turns ratio of n. The turns ratio (n) is defined as the ratio between the number of turns in the secondary winding (N_s) to the primary winding (N_p) ($n = \frac{N_s}{N_p}$). Additionally, a power inductor (L_{DAB}) is essential on the primary side of the DAB. The

power flow control concept of the DAB is derived from the power flow control between voltage nodes in high-power transmission lines in electrical power systems engineering [7], [12]. Figure 3 shows the DAB converter equivalent circuit, neglecting losses. To transfer power bidirectionally between the HV bus and the LV1 bus, time-varying voltages (v_1) and (v_2) must be applied to the inductor with a phase shift angle (ϕ). The voltage (v_2) is equal to the transformer's secondary voltage (v_3) when referred to the primary side ($v_2 = \frac{v_3}{n}$). A positive phase shift angle causes power to flow from the HV bus to the LV1 bus, while a negative phase shift angle causes power to flow in the opposite direction. The signals $u_1(t)$ and $u_2(t)$ represent the PWM signals for the primary and secondary H-Bridges, respectively, which are square waves with a 50% duty cycle in the case of single-phase shift (SPS) modulation.

SPS is the standard modulation technique for the DAB, where the control parameter is only the phase shift angle. However, other modulation techniques are mentioned in the literature, such as double phase shift (DPS), triple phase shift (TPS), extended phase shift modulation (EPS), triangular modulation (TRG), trapezoidal modulation (TRP), and variable frequency modulation (VFM) [13]. These techniques can improve the efficiency of the DAB in different operating regions, although they vary in implementation complexity. In this paper, SPS is considered in the evaluation of the concept.

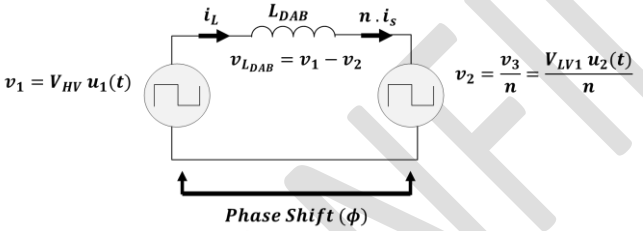

Fig. 2. DAB converter equivalent circuit with neglected losses.

B. *Design of DAB parameters*

Figures 4-5 show the key waveforms of the DAB converter in forward and reverse control modes at rated power conditions. The figures show at each switching cycle the current distribution between the MOSFET drain-source (i_S) path and body diode path (i_D). The positive notion of the current is shown in Figure 3. Equation 1 shows the power flow control equation as a function of the phase shift angle (ϕ), the converter switching frequency (f_{swDAB}), the inductance (L_{DAB}), the HV side voltage (V_{HV}) and LV1 side voltage (V_{LV1}) [12]. Equations 2 and 3 show the converter's average DC Input current (I_{HV}) and DC output current (I_{LV1}). Both of the components represent the average filtered value of (i_{HB1}) and (i_{HB2}) over one switching cycle ($T_s = \frac{1}{f_{sw}DAB}$) [3], [14].

$$P = \frac{V_{HV}\,V_{LV1}\,\phi\,(1-\frac{|\phi|}{\pi})}{2\,n\,\pi\,f_{swDAB}\,L_{DAB}} \quad (1)$$

The ratio between the phase shift angle and the half switching period (π) is known as the phase shift ratio ($d = \frac{\phi}{\pi}$). Equations 1 can be expressed in term of d, which represent the phase shift as time delay period ($T_\phi = \frac{d\,T_s}{2}$). This value can give more insight on the required simulation model minimum sampling time. The inductor design equation is shown in equation 2 by

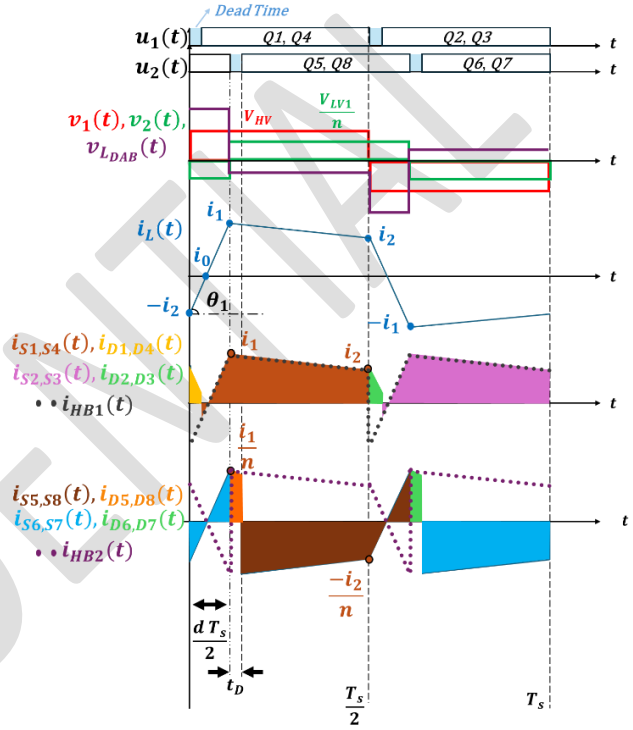

Fig. 3. DAB key waveforms in forward power control mode.

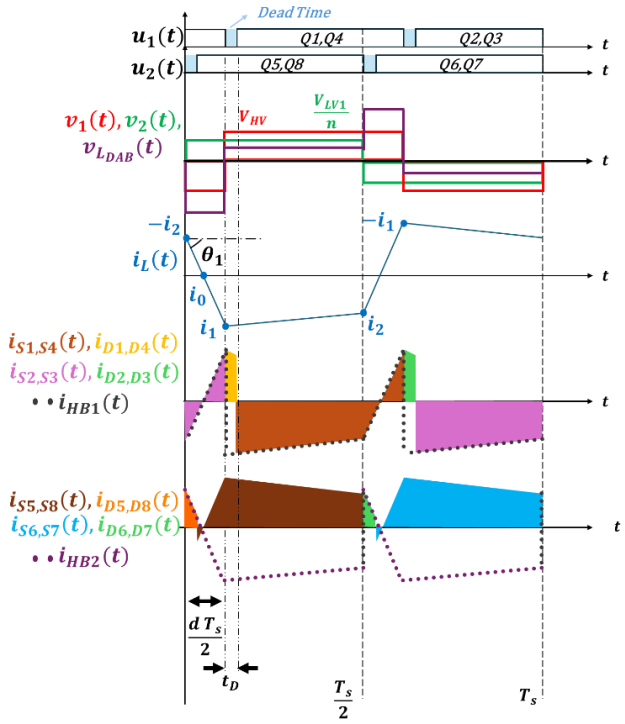

Fig. 4. DAB key waveforms in reverse power control mode .

rearranging equation 1 [13], [15]. Phase shift ratio (d) can be controlled in range $(-0.5 \le d \le 0.5)$, which correspond to phase shift range of $(\frac{-\pi}{2} \le \phi \le \frac{\pi}{2})$. The DAB converter average power versus the phase shift ratio can be seen in Figure 6. The max power transferred by the converter can be estimated as shown in equation 3.

$$L_{DAB\,Min} = \frac{V_{HV\,Min}\; V_{LV1\,Min}\; d_{max}\; (1-|d_{max}|)}{2\,n\,P_{max}\; f_{swDAB}\; L_{DAB}} \quad (2)$$

$$P_{max} = \frac{V_{HV}\; V_{LV1}}{8\,n\,f_{swDAB}\; L_{DAB}} \quad (3)$$

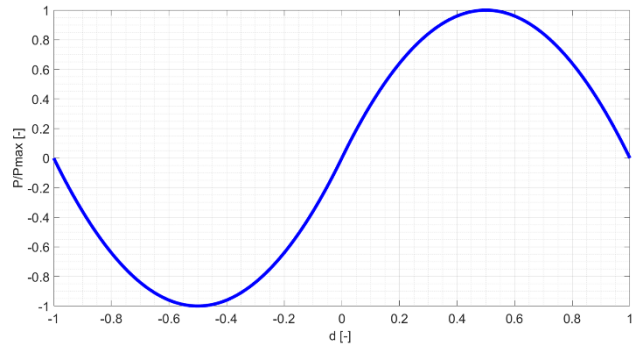

Fig. 5. Average power charcterization of DAB converter with respect to phase shift ratio (d) using SPS control.

Selecting the maximum rated phase shift angle (d_{max}) is crucial for designing the DAB converter controller and inductor. Increasing d_{max} requires a larger inductor and expands the zero voltage switching (ZVS) rang. However, it reduces system efficiency due to higher inductor RMS current. Conversely, reducing d_{max} improves efficiency but degrades the control loop. Limiting d_{max} to ±0.4 will avoid control loop non-linearity degradation as suggested in [3], [13].

The design of the DC link filter capacitor is essential to meet the EV maximum peak-peak ripple voltage requirements. Equations 4 and 5 show the design equations of the HV and LV1 DC link filter capacitors [15]. Δv_{LV1} and Δv_{HV} are the maximum allowed peak-peak ripple voltages.

$$C_{LV1} = \frac{V_{HV\,MAX}\; d_{max}^2}{4n\; f_{swDAB}^2\; L_{DAB}\; \Delta v_{LV1}} \left(\frac{d_{max}^2}{4} - d_{max} + 1\right) \quad (4)$$

$$C_{HV} = \frac{V_{LV1\,MAX}\; d_{max}^2}{4\,n\; f_{swDAB}^2\; L_{DAB}\; \Delta v_{HV}} \left(\frac{d_{max}^2}{4} - d_{max} + 1\right) \quad (5)$$

C. *Zero voltage switching (ZVS)*

The primary inductor AC current waveform plays a big role in ensuring the ZVS of the H-Bridges, and in defining the Switches conduction losses and the inductor and transformer copper losses and core losses. The expressions of the inductor currents (i_1) and (i_2) at the respective time instants $(t_1 = \frac{dT_s}{2})$ and $(t_2 = \frac{T_s}{2})$ can be defined as shown in equations 6 and 7 [16], [17]. Whereas, (i_0) represent inductor current zero crossing instant [17]. The slope of the inductor current during $(\frac{dT_s}{2})$ period (θ_1) can be used to determine the zero crossing instant of the inductor current as shown in equations 8-9.

$$i_1 = sign(d)\left(\frac{\left(V_{HV}\,(2|d|-1)\right) + \left(\frac{V_{LV1}}{n}\right)}{4\; f_{sw\,DAB}\; L_{DAB}}\right) \quad (6)$$

$$i_2 = sign(d)\left(\frac{V_{HV} + \left(\left(\frac{V_{LV1}}{n}\right)(2|d|-1)\right)}{4\; f_{sw}\; L_{DAB}}\right) \quad (7)$$

$$\theta_1 = \frac{2\; f_{sw\,DAB}\; (i_1+i_2)}{d} \quad (8)$$

$$t_{(i_0)} = \frac{i_2}{\theta_1} \quad (9)$$

To prevent short circuits in a half-bridge arrangement, a dead time period (t_D) must be introduced between the turn-off of one switch and the turn-on of its complementary switch. During this period, all four switches of an H-Bridge are off. Figures 8 show the dead time period for the primary H-Bridge. During this dead time period the following happens:

1. The drain-source capacitors (C_{ds}) of the turned-off switches (e.g., Q1, Q4) charge from 0 to V_{HV} , while the output capacitors of the switches to be turned on (e.g., Q2, Q3) discharge to 0. This called the resonance period of the H-Bridge as the energy is exchanged between C_{ds} and L_{DAB}.

2. Once the capacitors are discharged and the switch voltage is close to zero, the unparallel diodes (e.g., D2, D3) turn on if the inductor current direction is from source to drain (e.g., $i_2 > 0$), limiting the switch voltage to the diode forward voltage.
3. When the inductor current crosses zero (i_0), the current in the switch commutates from the diode path to the drain-source path (e.g., S2, S3).

These steps are repeated twice in each switching cycle at each H-Bridge, ensuring the anti-parallel diode is on before the switch turns on, and achieving ZVS.

The required dead time (t_D) is estimated by multiplying the switch's turn on/off times by a safety factor as shown in equation 10 [15]. Increasing the dead time increases the chance of achieving ZVS but also raises conduction losses due to the body diode, which has higher losses than the drain-source path. In the simulation, the dead time is set to a constant 100 ns, which is higher than the maximum voltage transient time for the SiC or Si MOSFET switches.

$$t_D = \frac{2\, v_{ds}\, C_{ds}}{i_{drain}} \tag{10}$$

The ZVS condition for DAB converter switches depends on the inductor current direction. ZVS is achieved when $i_2\, i_1 > 0$ [17]. Otherwise, hard switching occurs in one of the H-Bridges. Table 1 summarizes the ZVS conditions. This typically happens when the voltage ratio (M) deviates from the transformer

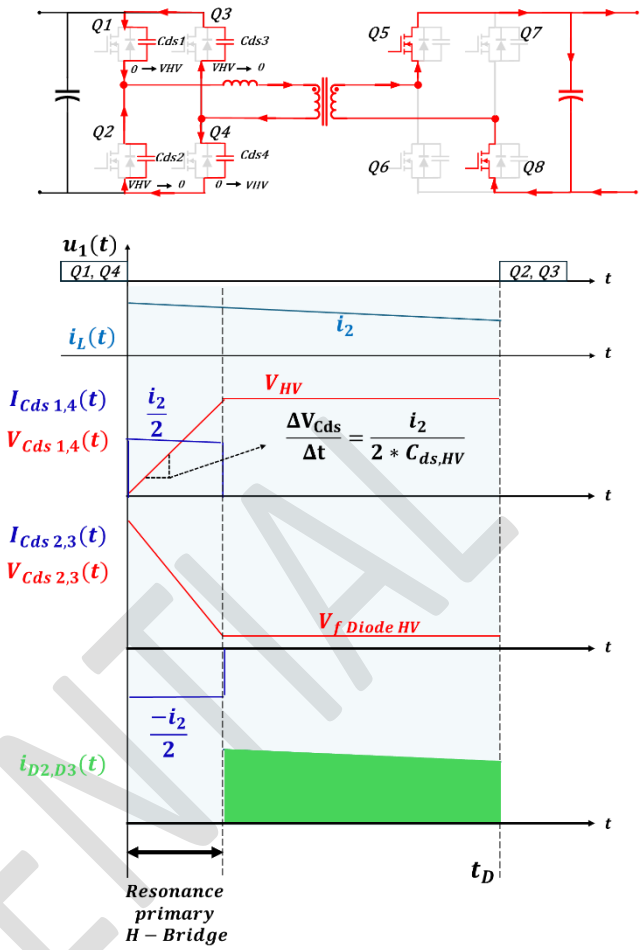

Fig. 6. DAB Primary H-Bridge Switching transients during switch

turns ratio. Equations 11-12 show the design of the transformer turns ratio (n) and the converter voltage ratio (M).

TABLE I. ZVS CONDITION FOR DAB CONVERTER WITH SPS MODULATION [17].

Mode	*Condition*	*Primary H-Bridge*	*Secondary H-Bridge*
Forward Power	$i_1 > 0$ *and* $i_2 > 0$	ZVS	ZVS
	$i_1 < 0$ *and* $i_2 > 0$	No ZVS	ZVS
	$i_1 > 0$ *and* $i_2 < 0$	ZVS	No ZVS

$$n = \frac{V_{LV1\ Nominal}}{V_{HV\ Nominal}} = \frac{48V}{700V} = \frac{N_s}{N_p} \tag{11}$$

$$M = \frac{v_{LV1}}{n\, v_{HV}} \tag{12}$$

The inductor currents i_1 and i_2 are influenced by the voltage ratio (M) and phase shift ratio (d). Equations 13 and 14 outline the ZVS conditions for the primary and secondary H-Bridges. Figure 8 shows the ZVS boundaries for voltage ratios from 0 to 2. In APM applications, the voltage ratio ranges from 0.7 (HV battery at 730V and LV1 battery at 36V) to 1.6 (HV battery at 550V and LV1 battery at 54V). If the phase

shift ratio is below 0.15, the primary and secondary H-Bridges will experience hard switching.

$$ZVS_{Primary}: d > \frac{M-1}{2M} \quad if \ M > 1 \qquad (13)$$

$$ZVS_{Secondary}: d > \frac{1-M}{2} \quad if \ M < 1 \qquad (14)$$

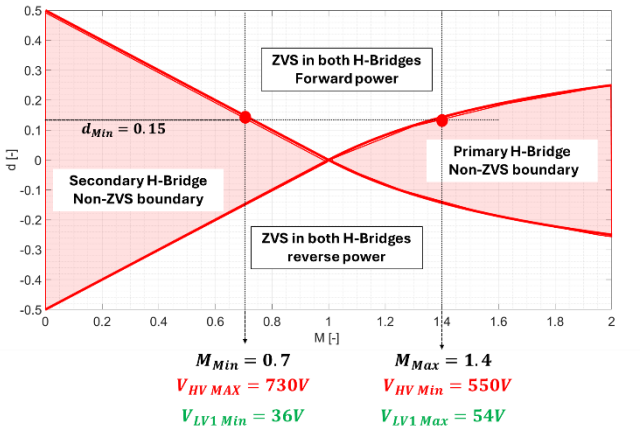

Fig. 7. DAB ZVS boundries with respect to voltage ratio (M) and phase shift ratio (d).

IV. DESIGN OF SYNCHRONOUS INTERLEAVED BUCK-BOOST CONVERTER

A. *Interleaved buck-boost converter operation*

Figures 9-10 show the key-waveforms of the buck-boost converter. The interleaved modulation technique uses switches Q9 and Q11 in a 180° phase shift. Controlling the duty cycle (D) regulates voltages and currents on the LV1 and LV2 buses. The buck-boost converter operates exclusively in continuous conduction mode (CCM).

Equation 17 shows the voltage gain of the converter in buck operating mode [18] . In equation 17 the effect of non- ideality of the switching devices and the inductors L_{Buck1} and L_{Buck2} are taken into consideration to determine the required Duty ratio. (r_{LBuck}) is the inductor parasitic resistance. V_{sd} is the GaN switch on state voltage and r_{ds} is the GaN drain-source on-sate resistance. Finally, R_{Load} is the load resistance ($R_{Load} = \frac{V_{LV2}^2}{P_{Buck}}$). Figure 18 show the change in output voltage with respect to the duty cycle with variation in the LV1 bus voltage.

$$Gain_{Buck} = \frac{V_{LV2}}{V_{LV1}} = \frac{D - \left(\frac{(1-D)V_{sd}}{V_{LV1}}\right)}{1 + \frac{(r_{LBuck} + r_{ds})}{R_{Load}}} \qquad (17)$$

Equation 18 shows the definition of the converter gain in boost mode [19]. In the boost mode the relation between the gain and the duty cycle is non-linear and can be divided into positive gain region and negative gain

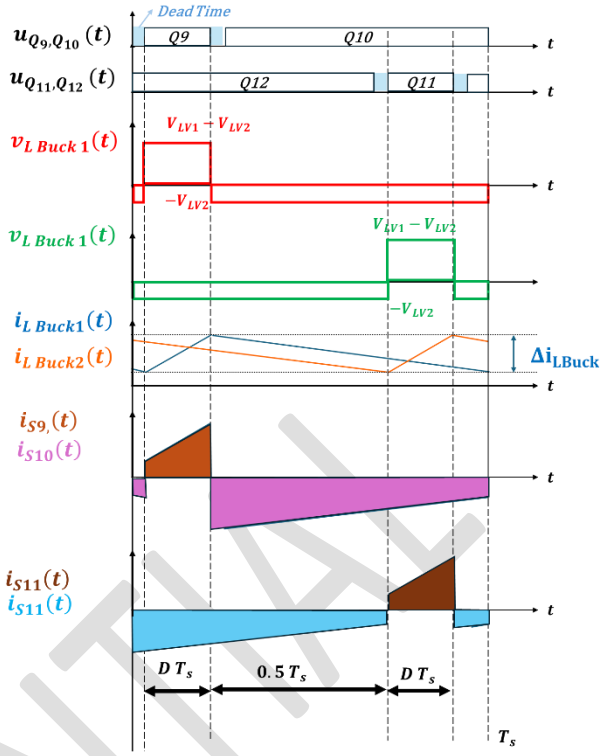

Fig. 8. Synchronous Buck-Boost converter key waveforms in buck control mode (Charging LV2 battery from LV1 bus).

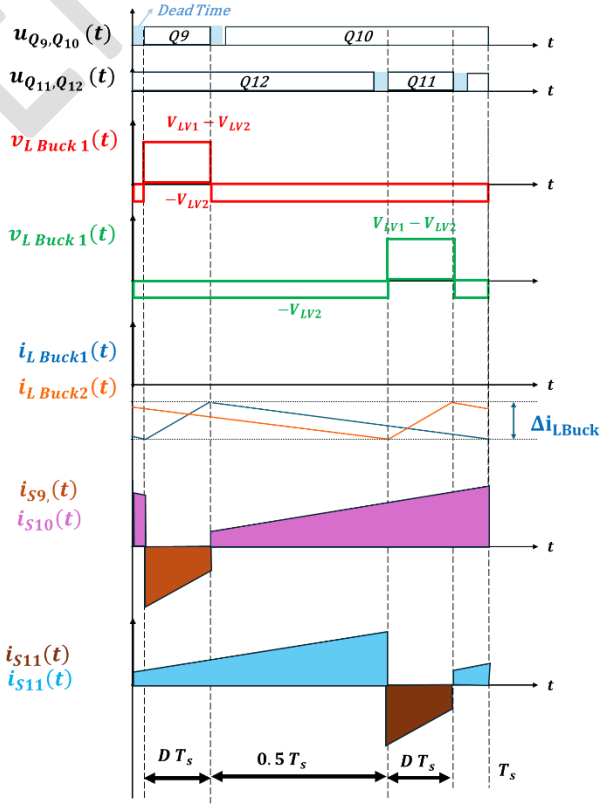

Fig. 9. Synchronous Buck-Boost converter key waveforms in boost control mode (Charging LV1 battery from LV2).

region. The boost converter is stable in positive gain region only [19]. Figure 19 show the change in the LV1 voltage with respect to D' for different load conditions. Where ($D' = 1 - D$) represent the duty ratio of the

complementary switches (Q10 and Q12) of the buck-boost converter. In boost mode $R_{Load} = \frac{V_{LV1}^2}{P_{Boost}}$.

$$Gain_{Boost} = \frac{V_{LV1}}{V_{LV2}} = \frac{\left(1-\left(\frac{D\,V_{sd}}{V_{LV2}}\right)\right) D\, R_{Load}^2}{((r_{LBuck}+r_{ds})\, R_{Load}) + D^2\, R_{Load}^2} \quad (18)$$

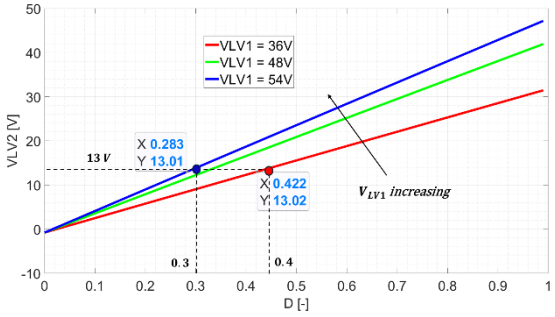

Fig. 10. Buck mode LV2 bus voltage variation with duty cycle at constant load of 3kW and with various LV1 bus voltages.

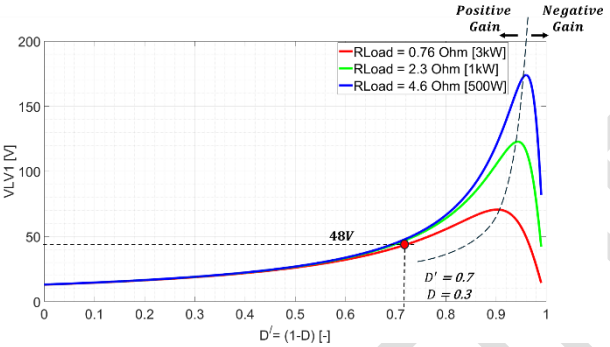

Fig. 11. Boost mode LV1 bus voltage variation with duty cycle at at various load with constant LV2 bus voltage of 12V.

B. *Design synchronouse Buck-Boost converter*

The main design parameters for the buck-boost converter are the inductors L_{Buck1} and L_{Buck2}, and the LV2 bus filter capacitor ($C_{out\,LV2}$). Inductor size limits the peak-to-peak ripple current (Δi_L) and the filter capacitor minimizes the peak-to-peak ripple voltage (Δv_{LV2}). L_{Buck1} and L_{Buck2} re designed to be the same size. Equation 19 shows the design equation for the two-phase buck converter [18], and equation 20 shows the design for the output filter capacitor [20], [21].

$$L_{Buck} = \frac{(1-D)V_{LV2}}{\Delta i_L\, f_{swBuck}} \left(1 + \frac{V_{sd}}{V_{LV2}} + \frac{r_{LBuck}+r_{ds}}{R_{Load}}\right) \quad (19)$$

$$C_{out\,LV2} = \frac{\Delta I_L}{8\, f_{swBuck}\, \Delta v_{LV2}} \quad (20)$$

V. Results and Analysis

A. *Co-Simulation Model*

Figure 13 shows the high-level co-simulation model of the APM. The circuit from Figure 3 is implemented in the PLECS-Blockset domain. An electrothermal model is created using datasheets of the SiC MOSFET, Si MOSFET, and GaN HEMT switches. A PI current controller for the DAB and buck-boost stages is implemented separately in the MATLAB SIMULINK environment. The APM efficiency is evaluated for two use cases:

1. Bi-directional power transfer between the HV bus and LV1 with only the DAB operating.
2. Buck and boost modes of the buck-boost converter with the DAB stage in constant power charging mode of 7kW.

Table 2 lists the simulation model parameters. The next subsection will discuss loss modelling in the PLECS-Blockset.

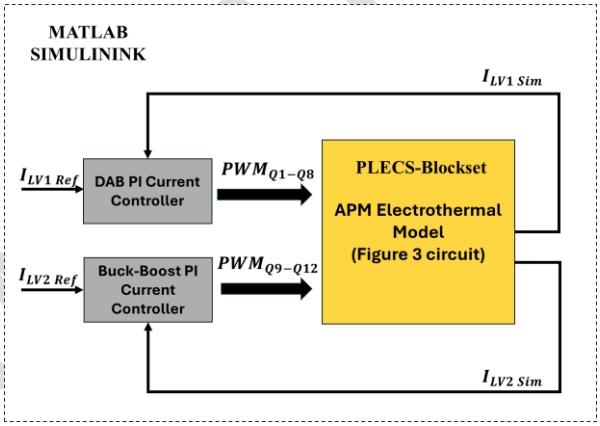

Fig. 12. APM co-simulation model.

TABLE II. PLECS-Blockset Simulation Model Parameters

Parameters	*Value*
HV Bus H-Bridge Semidocnductor Q1-Q4	SiC MOSFET 1700V / 75A (C2M0045170P)
LV1 Bus H-Bridge Semiconductor Q5-Q8	Si MOSFET 100V / 365A (IPTC014N10NM 5)
LV1/LV2 Buck/Boost semiconductor Q9-Q12	GaN HEMT 100V / 90A (EPC7018)
DAB stage switching frequency	50 kHz
DAB inductor parasistic resistance ($r_{L\,DAB}$)	5 mΩ
Buck-Boost stage switching frequency	500 kHz
DAB Inductor (L_{DAB})	90 μH
HV Bus Filter capacitor (C_{HV})	550 μF
LV1 Bus Filter Capacitor (C_{48V})	1.2 mF
DAB transformer Trurns ratio (Np:Ns)	43:3
Buck/Boost Input Filter Capacitor ($C_{Out\,LV2}$)	25 μF
Interleaved Buck/Boost Inductor ($L_{Buck\,1,2}$)	5 μH

B. *Losses Modelling*

In this paper, the considered losses are the Switches conduction and switching losses and the copper losses in the inductors and transformer parasitic resistances. Equations 21-23 detail the modeling of conduction losses in each switch of both converters. ($P_{Q-S\ cond}$) and ($P_{Q-D\ cond}$) represent

the conduction losses of the MOSFET and body-diode, respectively. The MOSFET's on-state resistance and the body-diode's forward voltage are modeled as lookup tables based on the switch junction temperature, switch voltage, and switch current.

The switching losses of the WBG switches (SiC MOSFET and GaN HEMT) are modeled using equations 24-26. ($P_{Q-S\ WBG\ Sw\ On/Off}$) represents the switching losses in the MOSFET. The body diode switching losses are neglected due to their minimal impact in WBG switches. The switching on and off energies (E_{on} and E_{off}) are provided as lookup tables in the datasheets.

The Si MOSFET datasheets do not provide a lookup table for the turn-on and turn-off energy losses. Additionally, the diode turn-on energies in the Si MOSFET must be considered [22]. Equations 27-31 detail the switching losses modeling for the Si MOSFET switches. (t_{ri}) and (t_{fi}) are the current rise and fall times in the MOSFET, while (t_{rV}) and (t_{fV}) are the voltage rise and fall times of the MOSFET. Q_{rr} represents the body-diode reverse recovery charge.

The copper losses in the DAB primary inductor and transformer are modelled using equations 32-33. The copper losses of the buck-boost inductor are modelled using equation 34.

$$P_{Q\ cond} = P_{Q-S\ cond} + P_{Q-D\ cond} \quad (21)$$

$$P_{Q-S\ cond} = \int_0^{T_s} r_{ds}\left(v_{ds}, i_s, T_j^o\right) i_s^2\, dt \quad (22)$$

$$P_{Q-D\ cond} = \int_0^{T_s} V_{sd}\left(i_D, T_j^o\right) i_D\, dt \quad (23)$$

$$P_{Q\ Sw\ WBG} = P_{Q-S\ Sw\ WBG\ On} + P_{Q-S\ Sw\ WBG\ Off} \quad (24)$$

$$P_{Q-S\ Sw\ WBG\ On} = E_{on}\left(v_{ds}, i_{ds}, T_j^o\right) f_{sw} \quad (25)$$

$$P_{Q-S\ Sw\ WBG\ Off} = E_{off}\left(v_{ds}, i_{ds}, T_j^o\right) f_{sw} \quad (26)$$

$$E_{On\ Q-S\ MOS} = v_{ds}\, i_s \frac{t_{ri}+t_{fV}}{2} + Q_{rr}.v_{ds} \quad (27)$$

$$E_{On\ Q-D\ MOS} = \frac{1}{4} Q_{rr}.v_{ds} \quad (28)$$

$$E_{Off\ Q-S\ MOS} = v_{ds}\, i_s \frac{t_{fi}+t_{rV}}{2} \quad (29)$$

$$P_{sw\ Q-S\ MOS} = \left(E_{On\ Q-S\ MOS} + E_{Off\ Q-S\ MOS}\right) f_{sw} \quad (30)$$

$$P_{sw\ Q-D\ MOS} = \left(E_{On\ Q-D\ MOS}\right) f_{sw} \quad (31)$$

$$P_{Cu\ LDAB} = I_{LDAB\ RMS}^2\, r_{L\ DAB} \quad (32)$$

$$P_{Cu\ Tf} = I_{LDAB\ RMS}^2\, r_{Tf\ Pri} + \frac{\left(I_{LDAB\ RMS}^2\, r_{Tf\ Sec}\right)}{n^2} \quad (33)$$

$$P_{Cu\ LBuck} = 2\, I_{LBuck\ RMS}^2\, r_{LBuck} \quad (34)$$

C. Simulation results of DAB stage

Figure 14 demonstrates the performance of the DAB converter's PI current controller in both forward and reverse power control modes. The main control parameter for the current is the phase shift ratio (d). The controller's effectiveness in maintaining desired current levels through varying power flow directions. Figure 15 shows the DAB converter's efficiency across various loads and voltage gains. The converter reaches up to 98% efficiency at a unity voltage gain (M=1) and M=1.4 with a rated current of 200A. However, efficiency drops to 95% at M=1.4 due to increased conduction losses, as shown in Figures 16 and 17. At low loads, efficiency further decreases to 95% and 93% for M=0.7 and M=1.4, respectively, due to hard switching losses. The APM the converter operates mainly at high currents for fast battery charging, maintaining high efficiency despite lower load drops.

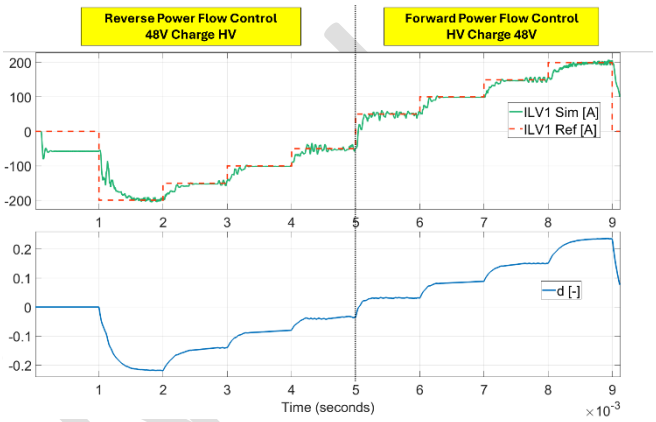

Fig. 13. DAB operation in forard power mode and revrese power mode.

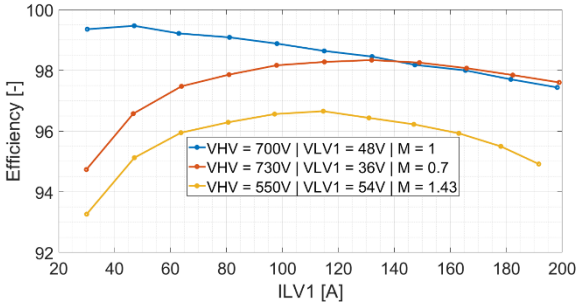

Fig. 14. DAB Efficiency at complet load range and different voltage gain values at stand alone mode.

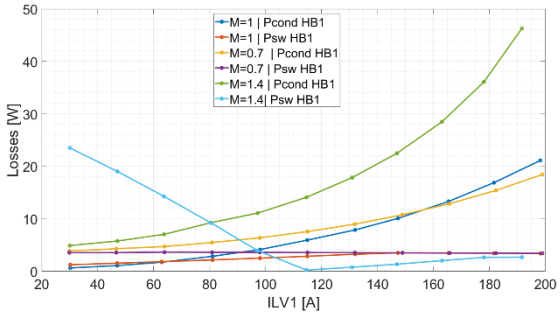

Fig. 15. DAB Primary H-Bridge (HB1) Losses at stand alone mode

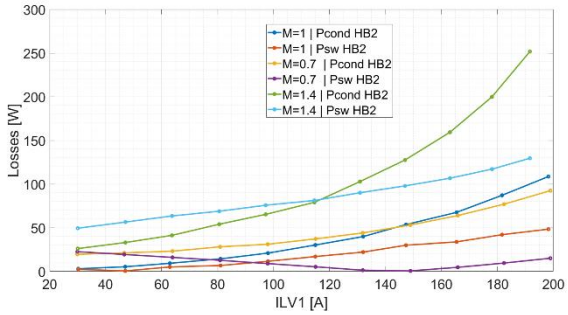

Fig. 16. DAB Secondary H-Bridge (HB2) Losses at stand alone mode

D. Simulation results of Buck-Boost stage

Figures 18-19 show the performance of the PI current controller for the buck-boost converter in both buck and boost modes. Figure 20 illustrates the converter's efficiency, peaking at 94% under a low load of 500W and decreasing slightly to 93% at a peak load of 3 kW. This efficiency is acceptable given the 12V load's relatively low percentage compared to the HV battery. The 12V network is mainly used for low-power applications like communication systems and onboard computers, which do not require significant power, thus justifying the observed efficiency levels.

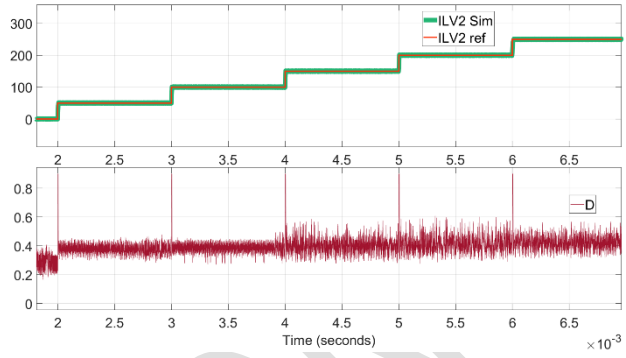

Fig. 17. Buck-Boost converter PI controller operation in Buck mode (LV1 charge LV2)

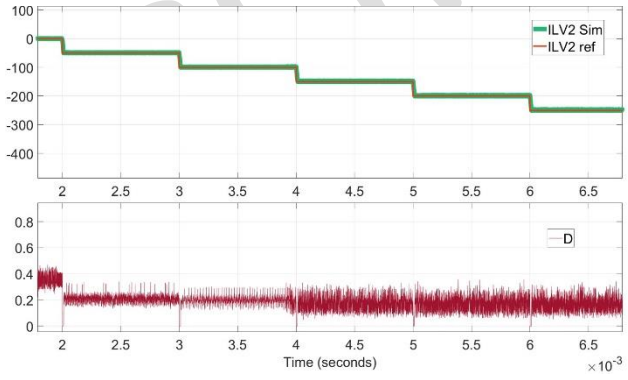

Fig. 18. Buck-Boost converter PI controller operation in boost mode (LV2 charge LV1)

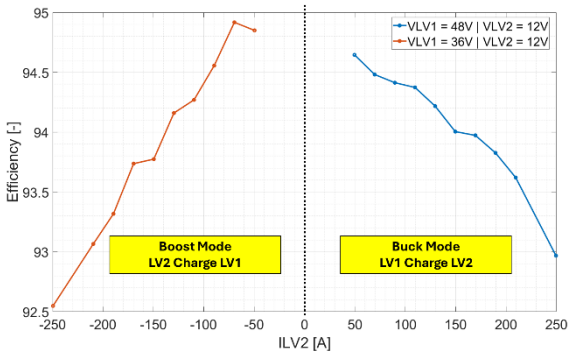

Fig. 19. Buck-Boost converter Efficiency at compleate load range while the DAB converter operate at constant power of 7 kW

VI. Conclusion

This paper presents the design and evaluation of an efficient bidirectional cascaded APM for electric trucks, using Si MOSFET, SiC MOSFET, and GaN HEMT technologies. The APM, transferring energy from a HV battery to LV batteries, achieves a peak efficiency of 98% at 10 kW. It features a two-stage topology: an isolated DAB converter for HV to 48V conversion, followed by a non-isolated synchronous interleaved buck-boost converter for 48V to 12V conversion.

Simulation results depict the DAB converter's high efficiency under various critical conditions. Efficiency drops at lower loads are noted due to switching losses. The buck-boost converter peaks at 94% efficiency at 500W and slightly decreases to 93% at 3 kW, suitable for 12V applications.

Overall, the APM design offers a robust and efficient solution for power distribution in electric trucks, highlighting the benefits of wide bandgap semiconductors for enhanced performance and efficiency.

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